Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A high density read-only memory (ROM) cell installed on a silicon substrate for storing data, comprising:
a first doped region being of a second conductive type installed on the silicon substrate;
a plurality of first heavily doped regions being of a first conductive type installed in the first doped region;
a second doped region being of the second conductive type installed on the silicon substrate; and
a gate installed on the surface of the silicon substrate and adjacent to the first doped region and the second doped region.

[c2] 2.The ROM cell of claim 1 installed in a doped well being of the first conductive type on the silicon substrate.

[c3] 3.The ROM cell of claim 1 wherein the first conductive type is P-type, and the second conductive type is N-type.

[c4] 4.The ROM cell of claim 1 wherein the first conductive type is N-type, and the second conductive type is P-type.

[c5] 5.The ROM cell of claim 1 wherein the first doped region is a drain doped region and the second doped region is a source doped region, and each of the plurality of heavily

doped regions and the first doped region form a diode so that a plurality of drain signals respectively passing through the plurality of heavily doped regions do not interfere with each other.

[c6] 6.A high density ROM cell installed on a silicon substrate for storing data, comprising:
a plurality of first doped regions being of a second conductive type installed on the silicon substrate;
a second doped region being of the second conductive type installed on the silicon substrate; and
a gate installed on the surface of the silicon substrate and adjacent to the plurality of first doped regions and the second doped region.

[c7] 7.The ROM cell of claim 6 installed in a doped well being of the first conductive type on the silicon substrate.

[c8] 8.The ROM cell of claim 7 wherein the first conductive type is P-type, and the second conductive type is N-type.

[c9] 9.The ROM cell of claim 7 wherein the first conductive type is N-type, and the second conductive type is P-type.

[c10] 10.The ROM cell of claim 6 wherein the second conductive type is N-type.

[c11] 11.The ROM cell of claim 6 wherein the second conduc-

tive type is P-type.

[c12] 12.The ROM cell of claim 6 wherein the plurality of first doped regions are drain doped regions and the second doped region is a source doped region, and the gate has at least one extension structure respectively located between one of the plurality of first doped regions and another first doped region so that a plurality of drain signals respectively passing through the plurality of first doped regions do not interfere with each other.